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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

NOVACEK, CHRISTY L

ART UNIT	PAPER NUMBER
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2822

DATE MAILED: 07/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/780,317

Applicant(s)

HARLE ET AL.

Examiner

Christy L. Novacek

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 7/2/04.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the communication filed February 17, 2004.

Claim Objections

Claims 3, 4, 6, 7, 14 and 15 are objected to because of the following informalities:

Claim 3 recites the limitation of “in which if present the initial layer is likewise applied to the substrate”. The phrase “in which if present” should be replace with “wherein”. Also in claim 3, the term “likewise” should be deleted because it renders the claim unclear as to whether or not the initial layer is deposited in a discontinuous manner, as the mask layer is deposited.

In claim 4, the word “preferably” should be deleted because it renders the claim unclear as to whether or not the claim is positively reciting the existence of a V- or U-shaped cross section.

Claim 6 recites the limitation of “the semiconductor material (5) is grown on using an ELOG technique.” A noun identifying onto what the semiconductor material is “grown on” should be inserted after the word “on”, or the word “on” should be deleted in order to have the claim make sense.

Similarly, claim 7 recites the limitation of “the semiconductor material (5) which has grown on has a substantially planar surface (7).” A noun identifying onto what the semiconductor material is “grown on” should be inserted after the word “on”, or the word “on” should be deleted in order to have the claim make sense.

Claims 14 and 15 are objected to because they are claims to the product of method claim 1 and the product can be made in other ways than that stated in the method claim. For example, the product can be made by depositing the semiconductor material (5) into the pits (41) by a

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CVD method instead of by using epitaxial deposition, as required in method claim 1. As is stated in MPEP section 608.01, “if claim 1 recites a method of making a specified product, a claim to the product set forth in claim 1 would not be a proper dependent claim if the product might be made in other ways.”

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 16, 18, 20 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 16 and 18 recite the limitation “wherein the plurality of semiconductor bodies are based on nitride compound semiconductor material.” It is unclear what the meaning of the term “based on” is in this limitation. Specifically, it is not clear whether “based on” is referring to the semiconductor bodies being formed on a lower support structure of a nitride compound, or if “based on” is referring to the semiconductor bodies being made of a starting formulation of a nitride compound.

Claim 20 recites the limitation of “said layer”. However, claims 17 and 19, upon which claim 20 depends, recites various “layers” including “a mask layer” “an underlying layer” and “a layer of semiconductor material”. Therefore, it is unclear as to which of these layers, “said layer” is referring.

Claim 21 recites the limitation of “said substantially planar surface”. There is insufficient antecedent basis for this limitation in the claim. Neither claim 21 nor claim 17, upon which claim 21 depends, recites any kind of planar surface.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4 and 6-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Koike et al. (EP 1263031, cited in IDS).

Regarding claim 1, Koike discloses forming a mask layer (4) over a substrate (1) or over an initial layer (20), such that the mask layer has a plurality of windows leading to the substrate or to the initial layer. A semiconductor material (32) that is to be grown onto the substrate in a subsequent method step substantially cannot be grown or can be grown to a significantly reduced extent onto the mask layer by comparison with the substrate or the initial layer. The substrate or the initial layer is etched back in the windows, in such a manner that pits are formed in the substrate or in the initial layer starting from these windows. Semiconductor material is grown onto the substrate or onto the initial layer, in such a manner that lateral growth is promoted and the semiconductor material initially grows primarily from the flanks of the pits toward the center of the pits where they form a coalescence region, so that defects in the substrate or in the initial layer which impinge on the flanks of the pits bend off toward the center of the pits in the semiconductor material, and then, starting from the windows, grows over the mask layer and in

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each case grows together over the mask layer between adjacent windows, where it forms a further coalescence region. A component layer sequence (104/105/106/107/108/109) is grown onto the semiconductor material (Fig. 1-2; para. 0030).

Regarding claim 4, Koike discloses that a cross section of the pits perpendicular to the plane of the substrate can be formed in a V shape (para. 0037).

Regarding claim 6, Koike discloses that the semiconductor material (32) is grown using an epitaxial lateral overgrowth (ELOG) technique (para. 0002).

Regarding claims 7 and 20, Koike discloses that the grown semiconductor material (32) has a substantially planar surface (Fig. 1E).

Regarding claim 8, Koike discloses that the mask layer can have a lattice-like or mesh-like structure (Fig. 10A).

Regarding claim 9, Koike discloses that the mask layer may be made of silicon nitride (para. 0042).

Regarding claim 10, Koike discloses that the semiconductor material (32) and/or the component layer sequence includes a compound of elements from the main groups III and V (para. 0002, 0052).

Regarding claim 11, Koike discloses that the semiconductor material (32) and/or the component layer sequence includes a nitride compound semiconductor material (para. 0002, 0052).

Regarding claim 12, Koike discloses that the semiconductor material (32) can include a composition selected from the system $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$, where $0 \leq x \leq 1$, $0 \leq y \leq 1$ and $x+y \leq 1$ (para. 0002).

Regarding claim 13, Koike discloses that the substrate can be made of silicon, silicon carbide, or sapphire (para. 0032).

Regarding claim 14, Koike discloses forming an electronic semiconductor body (para. 0051-0065).

Regarding claim 15, Koike discloses that the electronic semiconductor body is a radiation-emitting semiconductor chip, in particular a light-emitting diode chip or a laser diode chip (para. 0051-0065).

Regarding claims 16 and 18, Koike discloses that the plurality of semiconductor bodies are based on nitride compound semiconductor material.

Regarding claim 17, Koike discloses forming a mask layer (4) over an underlying layer (31), wherein the mask layer has a plurality of windows over the underlying layer, and wherein the underlying layer includes at least one of a substrate and an initial layer. Koike discloses etching, through the windows in the mask layer, pits in the underlying layer. Koike discloses depositing a semiconductor material (32) by growing the semiconductor material laterally from flanks of the pits in the underlying layer, wherein first coalescence regions are formed substantially in the center of each of the pits, wherein defects in the underlying layer which contact the sides of the pits propagate in said semiconductor material in a lateral direction toward the first coalescence regions, and growing the semiconductor material outward from the windows, as the windows become full of deposited semiconductor material, over the mask layer, wherein second coalescence regions are formed above the mask layer (Fig. 1-2; para. 0030).

Regarding claim 19, Koike discloses forming a layer of the semiconductor material above both the mask layer and the pitted underlying layer (Fig. 1E).

Regarding claim 21, Koike discloses growing a sequence of component layers (104/105/106/107/108/109) on the substantially planar semiconductor material surface (Fig. 2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koike (EP 1263031, cited in IDS) in view of Hageman et al. ("Improvement of the Optical and Structural Properties of MOCVD Grown GaN on Sapphire by an in-situ SiN Treatment", cited in IDS).

Regarding claim 2, Koike discloses that the growth of the semiconductor material is effected by means of metalorganic vapor phase epitaxy (para. 0033). Koike does not disclose all the specifics of the epitaxial process, neither does Koike disclose how the mask layer is formed on the underlying layer. Like Koike, Hageman discloses forming a mask layer of SiN over a substrate and then using MOCVD to epitaxially grow a Group III nitride compound over the mask layer (pg. 660). Hageman discloses in-situ depositing the SiN mask material on the substrate in an epitaxy reactor in such a manner that a discontinuous mask layer is formed, in which windows leading to the substrate are already formed during the deposition of the mask layer (pg. 660). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Hageman to form the SiN mask layer of Koike because Koike does not disclose any particular method of forming the mask layer and Hageman teaches a

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method of forming the mask layer that results in a stable SiN mask that allows epitaxial growth of a Group III nitride compound layer that has improved optical and structural properties.

Regarding claim 3, Koike discloses depositing the initial layer epitaxially, but does not specifically disclose depositing the initial layer in-situ in the epitaxial reactor. At the time of the invention, it would have been obvious to one of ordinary skill in the art to deposit the initial layer in-situ in the epitaxial reactor because by depositing the initial layer in-situ, the substrate can be protected from contamination which would result from transporting the substrate out of the reactor between deposition steps and because, by depositing the initial layer in-situ, fewer process steps are required and the method of Koike can thereby be carried out more efficiently.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koike (EP 1263031, cited in IDS).

Regarding claim 5, Koike does not specifically disclose that the semiconductor material (32) includes a plurality of layers of different compositions. However, Koike discloses forming a plurality of layers of different compositions over the semiconductor material. At the time of the invention, it would have been obvious to one of ordinary skill in the art to deposit the plurality of overlying layer of Koike of the same epitaxial growth process used to grow the semiconductor material (32) because Koike does not teach any particular method of depositing these plurality of overlying layers and because by depositing the plurality of overlying layers epitaxially in-situ, the substrate can be protected from contamination which would result from transporting the substrate out of the reactor between deposition steps and because, by depositing the plurality of overlying layers in-situ, fewer process steps are required and the method of Koike can thereby be carried out more efficiently.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:


Koike et al. (US 6,830,948) is the US Patent equivalent of EP 1263031, cited above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
June 16, 2005


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